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Electrostatic and Electrochemical Nature of Liquid-Gated Electric-Double-Layer Transistors Based on Oxide Semiconductors

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Abstract: The electric-double-layer (EDL) formed at liquid/solid interfaces provides a broad and interdisciplinary attraction in terms of electrochemistry, photochemistry, catalysts, energy storage, and electronics because of the large interfacial capacitance coupling and its ability for high-density charge accumulation. Much effort has recently been devoted to the fundamental understanding and practical applications of such highly charged EDL interfaces. However, the intrinsic nature of the EDL charging, whether it is electrostatics or electrochemistry, and how to distinguish them are far from clear. Here, by combining electrical transport measurements with electrochemical impedance spectroscopy (EIS), we studied the charging mechanisms of highly charged EDL interfaces between an ionic liquid and oxide semiconductor, ZnO. The direct measure for mobile carriers from the Hall effect agreed well with that from the capacitance−voltage integration at 1 Hz, implying that the pseudocapacitance does not contribute to carrier transport at EDL interfaces. The temperature−frequency mapping of EIS was further demonstrated as a "phase diagram" to distinguish the electrostatic or electrochemical nature of such highly charged EDL interfaces with densities of up to 8×10^{14} cm^{-2}, providing a guideline for electric-field-induced electronic phenomena and a simple method for distinguishing electrostatic and electrochemical charging in EDLTs not only based on a specific oxide semiconductor, ZnO, but also commonly applicable to all types of EDL interfaces with extremely high-density carrier accumulation.

Introduction

Electric field control of carrier density in a transistor configuration has been known as a powerful tool to tune the electronic states of condensed matter.[1] Recently, electric-double-layer transistors (EDLTs) using ionic liquids or electrolytes as gate dielectrics have attracted intensive attention[2−13] since the EDL, functioning as a nanogap capacitor with huge capacitance, can accumulate charges to a level as high as 8.0×10^{14} cm^{-2} at liquid/solid (L/S) interfaces.[12] This development triggered advancements in the electrostatic modulation of electron states at interfaces[10] such as electric-field-induced superconductivity on $SrTiO_3$ and ZrNCl.[3,4] In such a unique technique, the highly charged EDL interface is the central concept. Although the EDL has been known since the 19th century and is already widely used in various electrochemical cells such as lithium batteries, fuel cells, and energy storage elements,[14−16] to apply the EDL for tuning the physical properties of solid matter in a transistor configuration is a rather new issue. Particularly, in the fundamental physical understanding of EDL charging, for example,

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identifying the intrinsic nature of interfacial carrier accumulation, whether it is electrostatics or electrochemistry, and how to distinguish them are not yet clear.

In the present research, using a combination of electrochemical impedance spectroscopy (EIS) and transport measurement including the Hall effect, we investigated the charging dynamics and static charge accumulation of ionic-liquid/ZnO EDL interfaces in a transistor configuration. As the most direct physical way, the Hall effect is extremely helpful in evaluating mobile carriers at the interface,[11,12] whereas EIS clarifies the fundamental processes of the complicated interface chemistry.[17,18] The phase angle responses and resulting time domains in the EIS were established as a method for distinguishing the charging mechanisms and the electrostatic or electrochemical nature of EDL interfaces. The accumulated carrier densities n_s from EIS capacitance−voltage ($C-V_G$) integration were compared with n_s from the Hall measurements to quantitatively interpret the intrinsic nature of carrier accumulation. Temperature−frequency mapping of the EIS results, functioning as a "phase diagram" to distinguish varied charging mechanisms, provides solid proof that the EDL interfaces can be used as a physical tool for tuning the electronic states of solid matter.

Experimental Section

Atomically flat ZnO surfaces were obtained by annealing polished ZnO substrates (5×5 mm^2, Furuuchi Chemical Co.) at 1000 °C for 1 h. Ti/Au ohmic electrodes with a thickness of 30 nm/100 nm were evaporated on ZnO for a Hall-bar pattern with channel dimensions 500×200 μm. Au wires were bonded to the pattern, and the device was covered with SiO_2 except for the transport channel. The ionic liquid (IL) used in this study was mainly *N*,*N*-diethyl-*N*-(2-methoxyethyl)-*N*-methylammonium bis-(trifluoromethylsulfonyl)imide (DEME-TFSI) from Kanto Chemical Co. Other ILs with the same anion (−TSFI) were also used, such as *N*-methyl-*N*-propylpiperidinium (MPPR−), *N*,*N*,*N*-trimethyl-*N*-propylammonium (TPA−), 1,3-diallylimidazolium (AAIM−), 1-allyl-3-ethylimidazolium (AEIM−), and 1-ethyl-3-methylimidazolium (EMIM−). EDL charging processes were investigated in detail by electrochemical impedance spectroscopy using a Zahner Elektrik IM6eX impedance spectrum analyzer. On both Pt/IL/Pt and Pt/IL/ZnO sandwiched structures, the capacitance and EIS measurement were performed and the EDL capacitance, C_{EDL}, was derived from the equation $C_{EDL} = 1/(2\pi fZ'')$, where f is the frequency and Z'' is the imaginary part of the impedance. Note that the counter gate electrode is designed to have a much larger surface area than that of the working electrode. In this case, the additional reference electrode becomes unnecessary since most of the gate potential will drop at the working electrode interface, whether it is Pt or ZnO. The capacitance of the EDL formed at the gate electrode will be significantly large in the equivalent circuit, indicating that the measured EDL capacitance dominantly comes from the contribution of the EDL capacitor C_{EDL} at the working electrode. All electrical measurements were performed in a vacuum of about 10^{-1} Torr since the performance of EDLTs was found to be sensitive to both oxygen and humidity. The transport characteristics of all IL/ZnO-EDLTs were measured by a combination of a physical property measurement system (PPMS, Quantum Design) with an Agilent 5270B semiconductor parameter analyzer. The Hall effect measurement was carried out in the constant-current mode with a relatively large current of 1 μA to obtain a detectable Hall voltage for the instrument.

Applying an ionic liquid (DEME-TFSI) as the dielectric for EDLTs and using an oxide semiconductor (ZnO) with a high electron mobility of 100 cm^2/(V s) as the channel surface enables the realization of high-density carrier accumulation. So far, the maximum attainable sheet carrier density accumulated at the IL/ZnO interface is 8×10^{14} cm^{-2}, evaluated from the physical characterization, Hall measurement.[12] As a chemical method, the EIS measurement with an applied ac voltage of 5 mV and a frequency from 10 mHz to 1 MHz was performed in forms of frequency-dependent capacitance ($C-f$), impedance ($Z-f$), and phase angle ($\theta-f$), providing us with information on the static and dynamic charging parameters of the EDL interfaces[19−22] such as equilibrium charge concentrations, interfacial capacitance, and polarization relaxation time, τ_P.

Results and Discussion

Ideal EDL Charging without Interfacial Electrochemistry. To establish a standard scenario for electrostatic EDL carrier accumulation, the EIS measurement was first performed on a Pt/IL/Pt capacitor structure, which serves as an ideal EDL capacitor with minimal interfacial chemical processes. Normally, the equivalent electric circuit for such a sandwiched structure can be simply modeled as two resistor−capacitor (RC) circuits in series,[23,24] as shown in the inset of Figure 1a: one RC for the EDL interface (nanogap capacitance C_{EDL} of EDL and its resistance R_{EDL}) and one for the bulk IL (geometrical capacitance C_{IL} of bulk IL and its resistance R_{IL}). The specific values of these elements can be quantitatively described by fitting EIS results with the classical theory of impedance spectroscopy.[23,24] Importantly, the "time factor" for each RC circuit, defined as a time constant $\tau = 1/f = RC$ for charging dynamics, can be used as a fingerprint parameter to distinguish the nature of the EDL carrier accumulation because each RC circuit has its own specific frequency domain, which strongly depends on the charging mechanisms and can be directly identified from either the Bode plots (the $\theta-f$ and $Z-f$ plots) or the absolute values of the R and C elements.[25] On the basis of the observed oscillation of the phase angle with frequency, frequency domains corresponding to different types of capacitive behaviors can be identified.

Figure 1a shows the typical $\theta-f$ plots for the Pt/IL/Pt structure under various dc biases in terms of the phase angle as functions of the applied frequency. Since a pure capacitive behavior of an RC circuit always induces a response with a phase angle close to −90° and an impedance slope of −1, the phase oscillation, shown in Figure 1a, clearly indicates that there are two frequency domains, which correspond to two different types of capacitive behavior. The one in the frequency region above 100 kHz refers to a bulk IL capacitor with a small capacitance

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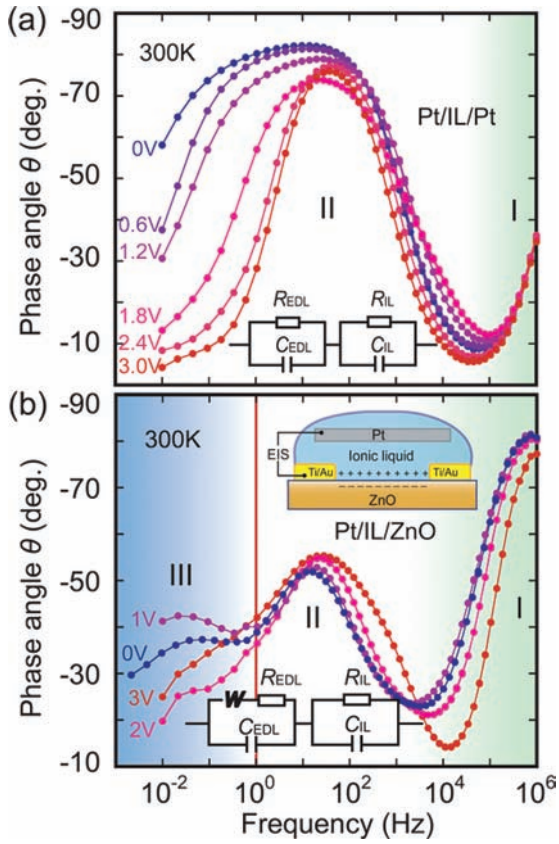

Figure 1. Comparison of room-temperature impedance spectroscopy between Pt/IL/Pt and Pt/IL/ZnO structures. (a) The $\theta-f$ plots in Pt/IL/Pt structure at varied dc biases. Inset: equivalent electric circuit, two resistor−capacitor (RC) circuits in series. Region I (green regime): bulk IL charging. Region II (white regime): electrostatic EDL charging. (b) Bode plot of ZnO EDLTs under bias. Region I (green regime): bulk IL charging. Region II (white regime): electrostatic EDL charging. Region III (blue regime): electrochemical pseudocapacitance charging. Upper inset: cross-section diagram of positively biased ZnO EDLT. Lower inset: equivalent electric circuit, two RC circuits in series and with additional Warburg impedance.

C_{IL} but a fast charging speed, which directly originates from the capacitance coupling in bulk IL between two Pt electrodes. The other one in the frequency range from 100 kHz down to 10 mHz corresponds to a typical EDL capacitor, resulting from the formation of EDLs at electrode surfaces. As shown in Figure 1a, the EDL phase angle at low frequency starts to decrease as dc bias (V_G) increases, indicating the resistive behavior in the interface. At the same time the peaks shift slightly toward high frequency and become more symmetric against log(f). The voltage-induced tunneling current (or leak current passing through the EDL interface), which can be reflected from the low-frequency impedance decreasing with increased dc bias, is supposed to be the origin of the bias-dependent behaviors of the phase angle and impedance since the quantum effect cannot be ignored any more due to the nanoscaled thickness of EDL.[26,27] However, in the case of electrostatic charging in the Pt/IL/Pt structure, only two domains (the EDL capacitor and the bulk IL capacitor) can be observed in the frequency region from 10 mHz to 1 MHz.

Interfacial Electrostatics and Electrochemistry. In contrast with the two phase regimes in the electrostatic charging of Pt/IL/Pt case mentioned above, from the phase angle response of the Pt/IL/ZnO structure (cross-section diagram and $\theta-f$ plot are shown in Figure 1b, one more frequency domain (Region III) can be clearly observed below 1 Hz. On the basis of these observations, we divided the whole frequency region in the Bode plot of IL/ZnO EDLTs into three independent parts:[25] (I) bulk capacitance above 10 kHz, which corresponds to the polarization of the bulk IL between the gate electrode and channel surface; (II) EDL capacitance in the frequency range from 10 kHz to 1 Hz, which refers to the EDL polarization at the confined interface; and (III) the chemically related pseudocapacitance below 1 Hz, which is supposed to be induced by chemical processes at the IL/ZnO EDL interface and behaves as a pseudocapacitance. The possible origins of these phase responses stem from the surface electrosorption of unavoidable impurities in the IL, such as H_2O, on ZnO surfaces[28,29] (discussed later). Note that the frequency of 1 Hz is the critical frequency to separate the electrostatics from the electrochemical regions in this particular system at 300 K.

After modeling the interfacial charging, the transport measurements were carried out on an EDLT with Pt/IL/ZnO sandwiched structures. The inset of Figure 2a shows the transfer characteristics of such an EDLT. One can clearly see the typical n-type transistor operation with electron accumulation at positive gate bias. The hysteresis-free transfer characteristics, measured with a source-drain voltage $V_D = 0.1$ V, show that the On−Off ratio of source-drain current I_D is about 100 within the operation voltage range of ±3 V and that the maximum current at gate voltage $V_G = 3$ V is as large as 170 μA, both of which directly reflect the highly charged behavior of the IL-EDLT.[11,12]

The frequency profile of the specific capacitance in the Pt/IL/ZnO structure, shown in Figure 2a, also consistently fits the categorization of the charging mechanisms at three different frequency regions. The specific capacitance shows a small value of 10 nF/cm^2 at high frequency (>100 kHz, bulk IL capacitance) and increases dramatically to values above 10 μF/cm^2 at frequencies lower than 1 kHz. The frequency increment (at which frequency the capacitance starts to increase) is basically determined by the time constant $\tau = 1/f = R_{IL}C_{EDL}$, which is strongly dependent on the device configuration, such as the size of the channel and the dielectric thickness. If the liquid dielectric between the gate electrode and ZnO channel can be as thin as 1−10 μm, like those using inkjet printing technique, which gives a much smaller resistance R_{IL} of IL, the capacitance starts to increase at a higher frequency and fast switching devices will be achieved. This is critically important for the high-frequency response. When the frequency decreases to 1 Hz, the capacitance gradually goes up to 30 μF/cm^2 (EDL capacitance). However at lower frequency, from 1 to 0.01 Hz, the capacitance involving interfacial chemical processes shows an accelerative increase rather than a constant, leading to a very huge capacitance value of more than 100 μF/cm^2.

To clarify the origins of such low-frequency phase angle responses, V_G dependence of capacitance was measured at

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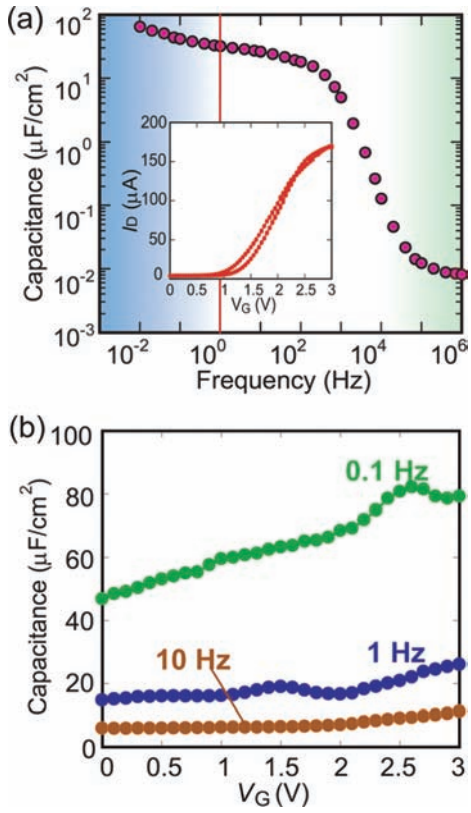

Figure 2. (a) Effective capacitance as a function of applied frequencies. The frequency regime for varied charging mechanisms is consistent with the frequency-dependent phase angle. Green regime (I): bulk IL charging. White regime (II): electrostatic EDL charging. Blue regime (III): pseudocapacitance charging. Inset: Typical transfer characteristics of IL/ZnO EDLTs with Hall-bar geometry, measured with a source-drain voltage V_D of 0.1 V. (b) Effective capacitance as a function of applied biases at 0.1, 1, and 10 Hz.

several frequencies around the critical value, shown in Figure 2b. At 1 and 10 Hz (in region II), the capacitance displayed weak V_G dependence, which is similar to the electrostatic behavior of solid dielectrics. The capacitance at 0.1 Hz, on the other hand, considerably increases with increasing V_G. The stronger V_G-dependent behavior at 0.1 Hz is suggestive of a dominating contribution of the pseudocapacitance. For an electrochemical interface, Faradaic charges (Q_F) transferred through EDL interfaces in an electrosorption process or in a surface redox process are always a function of gate potential. The derivative, dQ_F/dV, then causes additional capacitance: $C_{ps} = dQ_F/dV$. Such a capacitance is chemical in origin, referred to as pseudocapacitance, and can be well described by a phenomenological relationship: $C_{ps} = (1/2)\sigma^{-1}f^{-1/2}$ (σ is a parameter related to the Warburg impedance).[14–16,25] In contrast to the EDL capacitor operating in an electrostatic way, the pseudocapacitance accumulates charges in a slow way through Faradaic charge-transfer processes, where the effective capacitance can keep increasing with the decreased frequency.

Figure 3 shows a comparison of static charging states estimated from Hall measurement and $C-V_G$ integration. As indicated by the red curve, the sheet carrier density n_s from the Hall effect increases linearly with V_G, and the maximum attainable n_s is 5.4×10^{14} cm^{-2} with a V_G of 3 V at room temperature, which directly results in the high conductance in transistor performance shown in the inset of Figure 2b. In contrast with the Hall effect for estimating the number of mobile carriers, integration of the $C-V_G$ plot (blue curve) can be used for evaluating the total amount of accumulated charges using

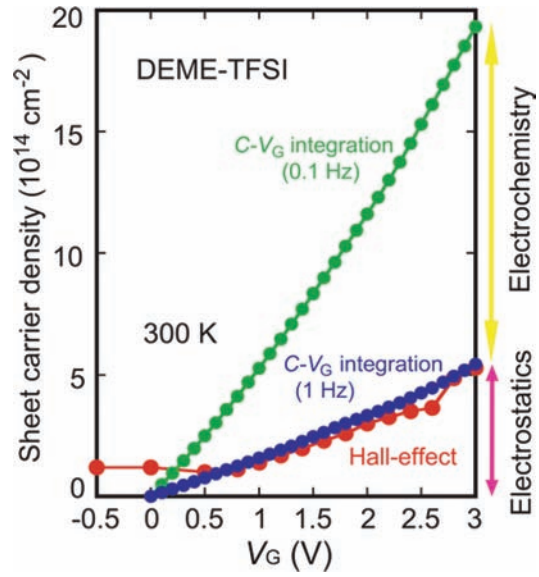

Figure 3. Comparison of static charging states in IL/ZnO EDLTs estimated from Hall measurement and the $C-V_G$ integration. (a) Interface charge densities as a function of V_G from Hall measurement (red dots) and from the $C-V_G$ integration (blue dots for 1 Hz and green dots for 0.1 Hz).

$Q_T = \int C dV_G = n_s eA + Q_F$, where Q_T is the total charge, Q_F is the Faradaic charge, $Q_H = n_s eA$ is the mobile charge, and A is the channel surface area. Since the effective capacitance is frequency dependent, the total charges estimated from the $C-V_G$ integration resultingly shows frequency-dependent behavior. Apparently, if the frequency enters the pseudocapacitance region, the charge estimation from $Q_T = n_s eA + Q_H$ will be much larger than that from the Hall measurement because of the Faradaic charges Q_F. On the other hand, the Q_F at and above 1 Hz can be neglected and, therefore, the total charges $Q = \int C dV_G$ will be equal to the mobile charges $Q_H = n_s eA$. The variation in the Q values estimated at 0.1 and 1 Hz (the value at 1 Hz agrees with that from the Hall effect) indicates that the Faradaic charges are chemically trapped at the interface and have no contribution to carrier transport in the channel. Consequently, the quantity of the chemically related charges Q_F can be quantitatively estimated from the variation between the Hall measurement and the $C-V_G$ integration at low frequency, as shown in Figure 3, providing a new quantitative method for understanding the interface electrochemistry.

Apparently, the quantity of the chemically related charges Q_F can be accurately evaluated from the variation between the Hall measurement and $C-V_G$ integration, providing a new quantitative method to understand the interface electrochemistry. As indicated in Figure 3, at the IL/ZnO EDL interface at $V_G = 3$ V, the total electrons from $C-V_G$ integration at 1 Hz is 5.4×10^{14} cm^{-2}, which is in agreement with the n_s value for the mobile electrons obtained from Hall measurement, indicating the electrostatic nature of interface charging, whereas at 0.1 Hz, the n_s from $C-V_G$ integration at $V_G = 3$ V is as high as 19×10^{14} cm^{-2} due to the accumulation of Faradaic charges. The density of the chemically related charges can be directly confirmed from the variation of these two values, namely, 13.6×10^{14} cm^{-2}, which means 0.33 electron per ZnO. These results tell that 1 Hz is the lowest frequency for an electrostatic EDL polarization without the occurrence of the pseudocapacitance. This means that the closer to 1 Hz the frequency is approached from the higher frequency, the more sufficient the EDL polarization relaxation. Otherwise, the ions of ILs, which are supposed to be fully polarized, will not relax to a saturated situation.

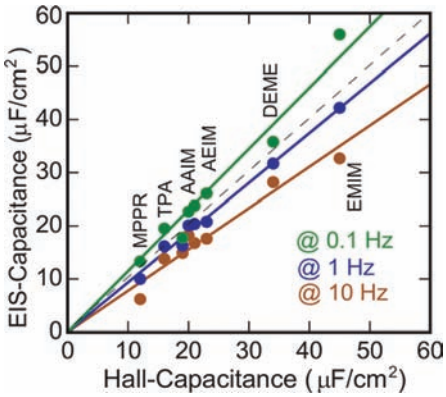

Figure 4. Comparison of EIS capacitance and Hall capacitance in ZnO EDLTs gated by varied ILs with the same TFSI anion. Dashed line indicates $C_{EIS} = C_{Hall}$. Solid lines are linear fitting lines for the capacitance at different frequencies.

For example, when we use the integration of the $C-V_G$ curve at 10 Hz to evaluate the accumulated carrier density, the value will be underestimated because of the insufficient polarization.

To confirm the generalization of the electrostatic nature of EDL charging, we measured various ILs and compared the Hall capacitance C_H and the EIS capacitance C_{EIS} of ZnO EDLTs. Figure 4 shows the related comparison between the C_H and the C_{EIS} at different frequencies. By using the equation $Q_H = n_s eA = C_H \Delta V A$, we can get the effective Hall capacitance, $C_H = (n_s/\Delta V)e$, from the slope $(n_s/\Delta V)$ of the linear n_s-V_G curve. Note that for all the tested ILs, the frequency of 1 Hz serves as the critical point to separate the electrostatic and electrochemical processes since the case of 1 Hz is closer to the dashed line, which indicates the exact situation of $C_{EIS} = C_{Hall}$. The EIS capacitance at 0.1 Hz is larger than the Hall capacitance but smaller than that at 10 Hz, implying that the chemically trapped carriers in the pseudocapacitor cannot be detected by the Hall measurement and have no contribution to the charge transport at the EDL interface. These observations mean that the phenomena described in Figure 2 are widely applicable to other L/S EDL interfaces.

"Phase Diagram" for Electrostatics and Electrochemistry. Figure 5a shows the temperature−frequency mapping for the phase angle of EIS, demonstrating a "phase diagram" to distinguish the charging mechanisms and the electrostatic/electrochemical nature of EDL interfaces. In this two-dimensional mapping, three independent regions that correspond to varied charging mechanisms can be recognized by clear boundaries, which are defined by using the valley points in the $\theta-f$ plots at each temperature and are marked with yellow lines. One can see that this mapping demonstrates two paths to make EDLTs work in an electrostatic mechanism: high frequency or low temperature. Although electrochemical charging might coexist with the electrostatic case near room temperature, it can be avoided by selecting a higher working frequency for the EDL interface.[2,13] Another path is at low temperature, because with decreasing temperature, the phase angle peak for pseudocapacitance gradually shifts to a lower frequency, finally going beyond the measurable limit of 10 mHz below 250 K. In other words, only the frequency domains corresponding to electrostatic charging processes (the EDL and bulk IL charging) remain measurable below this temperature, implying that the chemical interfacial processes can be practically neglected in low-temperature charging even though it still could occur kinetically at an extremely slow rate. This "phase diagram" provides us with a guideline for practical device applications with electrostatic interfacial processes.

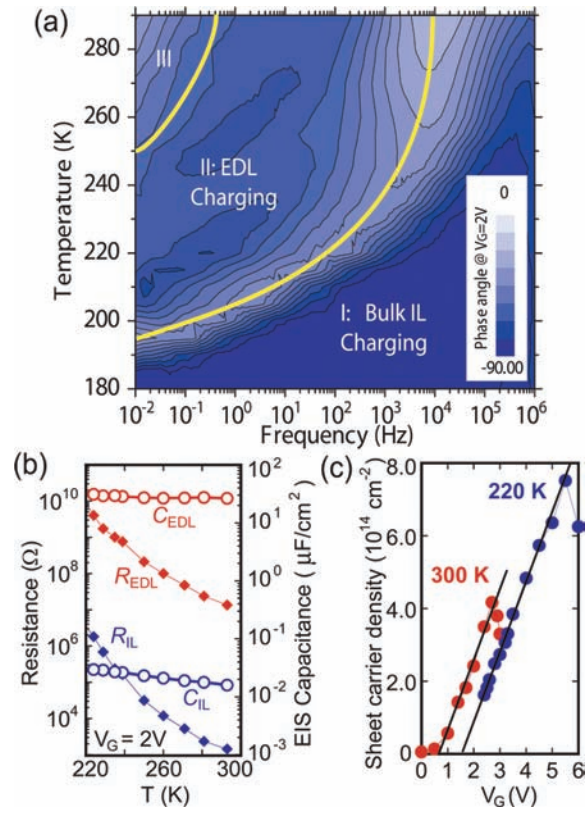

Figure 5. (a) Temperature−frequency mapping for the phase angle of the Bode plot. The yellow curve, drawn by using valley points of phase angles, is the critical boundary to distinguish three charging mechanisms. (b) Temperature-dependent charging parameters in the equivalent circuit of IL/ZnO EDLTs, deduced by fitting the Cole−Cole plots. (c) Comparison of V_G-dependent sheet carrier density at 300 and 220 K. The slope indicates Hall capacitance.

Figure 5b shows the temperature-dependent behaviors of the RC elements in equivalent circuits whose values were obtained by fitting the Cole−Cole plots. One can see that R_{IL} and R_{EDL} exponentially increase with decreasing temperature, whereas capacitance C_{IL} and C_{EDL} are almost invariant with temperature. Such weak temperature dependence of C_{EDL} is quite different from the rapid decrease of pseudocapacitances by cooling but similar to that of solid dielectrics, directly suggesting the electrostatic nature of EDL charging. Meanwhile, the Hall measurements at different temperatures shown in Figure 5c also proved a solid-dielectric-like behavior of liquid-gated EDLTs. Since the slope $(n_s/\Delta V)$ is almost parallel between 300 and 220 K, the Hall capacitance $C_H = (n_s/\Delta V)e$ (around 30 μF/cm^2) was almost independent of temperature, being consistent with the values in Figure 5b. In such a case, high-density carrier accumulation in a pure electrostatic mode can be effectively achieved at low temperature, which is very helpful for the electrostatic tuning of electronic states at EDL interfaces.

Polarization Dynamics of Electrostatic EDL Charging. In the Debye model with a single time constant, the dielectric loss ε'' has been widely used for the characterization of polarization relaxation processes, and the dielectric relaxation can be expressed as

$$\varepsilon - \varepsilon_\infty = \frac{\varepsilon_s - \varepsilon_\infty}{1 + \omega^2\tau^2} - j\frac{\omega\tau(\varepsilon_s - \varepsilon_\infty)}{1 + \omega^2\tau^2}$$

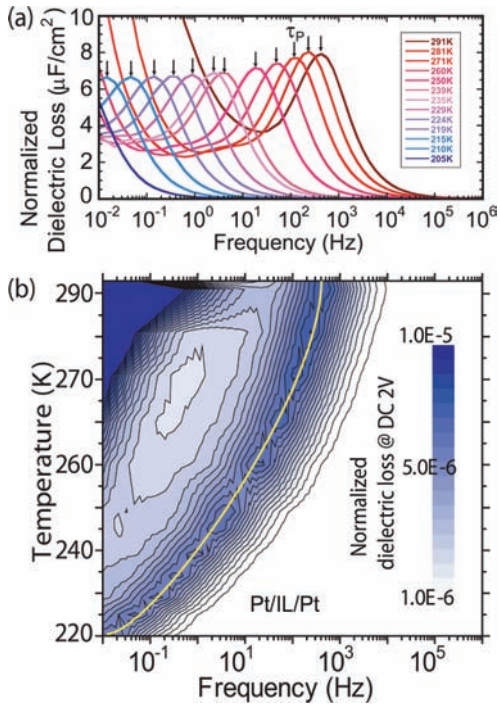

Figure 6. (a) Capacitance loss $(\varepsilon_0/d)\varepsilon''$ spectra of highly charged interfaces at varied temperatures. Arrows: peak frequencies of spectra. (b) Temperature−frequency mapping for the dielectric loss of EDL charging, another type of "phase diagram" for recognizing the electrostatic EDL charging. Yellow line: peak frequencies of polarization relaxation time τ_P of EDL charging.

where the real and imaginary parts of this expression are the Debye relaxation relations. Since in the liquid dielectric case, we do not know the exact thickness of the EDL capacitor, we normalized the Debye model with a factor ε_s/d. Figure 6a shows the frequency-dependent capacitance loss $(\varepsilon_0/d)\varepsilon''$ (normalization of dielectric loss by the factor ε_0/d) at temperatures from 290 K down to 205 K. The $(\varepsilon_0/d)\varepsilon''$ is symmetric about a central frequency with a characteristic shape and width, from which the polarization relaxation time for EDL can be obtained by using $\tau_P = 1/f = 2\pi/\omega$. This suggests that the EDL charging at the L/S interfaces satisfies the Debye relaxation relationship well. Figure 6b shows the temperature−frequency mapping for the capacitance loss $(\varepsilon_0/d)\varepsilon''$, from which the temperature-dependent behavior of the τ_P in the EDL charging process can be expressed by the yellow line. Varied blue areas, which were isolated by the "valley" zones, stand for different polarization relaxation mechanisms, which also can help us to recognize the electrostatic EDL capacitance (Region II). Consistent with observations in Figure 5a, with temperature cooling to 250 K, only the polarization relaxation for EDL exists in the measurable frequency region. In such a case, a pure electrostatic EDL carrier accumulation can be effectively achieved at low temperature for tuning electronic states or realizing new electronic phenomena.

The capacitance loss (the imaginary part of capacitance $(\varepsilon_0/d)\varepsilon''$), shown in Figure 6, is symmetric about a central frequency with a characteristic shape and width, indicating that the EDL charging agrees well with the Debye relaxation relationship, which is the basic model for electrostatic polarization in solid dielectrics.[28,29] From the central frequency, the polarization relaxation time of the EDL can be obtained by using $\tau_P = 1/f$. The observed τ_P changes over 4 orders of magnitude (from several milliseconds at room temperature to a hundred seconds at low temperature) because of various charging mechanisms. Basically, this behavior is explained in the framework of the thermally activated process of $\tau_P = \tau^* \exp(E^*/kT)$. Figure 7 shows the Arrhenius plot for several relaxation times in which $\tau_{ch} = R_{IL}C_{EDL}$ (red curve), τ_P (blue curve) for the Pt/IL/Pt structure, and τ_P for the Pt/IL/ZnO structure (black curve). The plots for both structures exhibit the same slope (dashed line) in the low-temperature region, suggesting that they have almost the same activation energy (810 meV) and, therefore, the same charging nature at low temperature even though the slopes at higher temperatures change possibly due to the contributions of a variety of electrochemical reactions specific to oxide surfaces. This is another piece of evidence showing that pure electrostatic charging occurs in the low-temperature regime, where chemical reaction is dramatically suppressed. Consistent with observations in Figure 5a, with temperature cooling to 250 K, only the polarization relaxation for EDL exists in the measurable frequency region. In such a case, a pure electrostatic EDL carrier accumulation can be effectively achieved at low temperature for tuning electronic states or realizing new electronic phenomena.

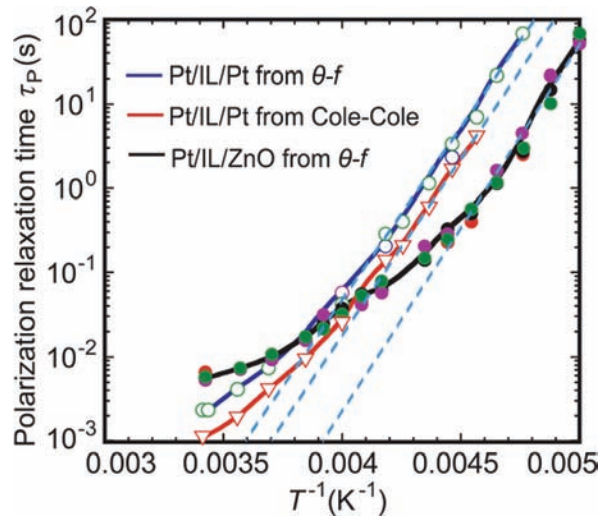

Figure 7. Arrhenius plot of polarization relaxation time τ_P as a function of T^{-1}. Open squares: τ_P from the capacitance loss spectra of the Pt/IL/Pt structure. Triangles: calculated values of $\tau_{ch} = R_{IL}C_{EDL}$ for the Pt/IL/Pt structure. Filled circles: τ_P from the capacitance loss spectra of the Pt/IL/ZnO device. Dashed lines: linear fit of curves for extracting activation energy.

Conclusions

With a combination of EIS and Hall measurements, we investigated charging mechanisms in the EDL transistor, which has an emerging capability for the electrostatic tuning of the electronic properties of matter. The direct measure for mobile carriers from the Hall effect agreed well with that from the capacitance−voltage integration at 1 Hz, implying that the pseudocapacitance does not contribute to carrier transport at EDL interfaces. The temperature−frequency mapping of EIS was further established as a "phase diagram" to distinguish the electrostatic or electrochemical nature of such highly charged EDL interfaces with densities of up to 8×10^{14} cm^{-2}. We demonstrated a simple method for distinguishing electrostatic and electrochemical charging in EDLTs based on a specific oxide semiconductor, ZnO, but this is commonly applicable to all types of EDL interfaces with extremely high-density carrier accumulation.

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